Architecture and Performance Overview of a Highly Integrated 13x13mm Single-Package Radio (SPR) Module for Dualband EGSM900 / GSM1800 Applications

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Abstract **– The RF system architecture and the performance overview for a very highly-integrated Single Package Radio (SPR) module for dual-band EGSM900/GSM1800 applications is presented. The module realizes all the RF functions required for the dual-band GSM application. These functions as well as their implementations are described. The integrated LO generation consists of reference oscillator circuitry, a UHF oscillator, and delta-sigma fractional-N synthesizer. The receiver is based on a direct-conversion (zero-IF) architecture with the front-end selectivity performed by the two integrated SAW filters. The transmitter is comprised of an upconversion-loop transmit chain with two high-power transmit oscillators, a dual-band power amplifier, detector-based transmit power control, transmit/receive switch, duplex filter and all other necessary filters. Diverse die technologies are utilized to apply the optimum process for each function. The SPR module is implemented on a low cost 4-layer laminate substrate and overall dimensions are 13x13x1.8 mm. Measured results against GSM specifications are presented.**

I. INTRODUCTION

Advances in transceiver design for the purpose of integration have recently made possible a great reduction in the physical size of the RF section of the typical cellular handset. In the GSM area, this has come about through the integration of several key circuit blocks which previously had existed only as discrete components. Such integration has required not only new circuit development but development of radio system architectures either diverging from the traditional, or made newly practical by the use of self-correction techniques.

Here the integration of the GSM handset transceiver is taken a step further, where a single-package radio is made practical by the aforementioned integration. In this paper we describe the RF architecture of a dual-band (EGSM900/GSM1800) single-package radio, which provides all RF functions required in a GSM handset from baseband signals to the antenna.

II. PHYSICAL ATTRIBUTES

The SPR module is shown in Fig. 1.

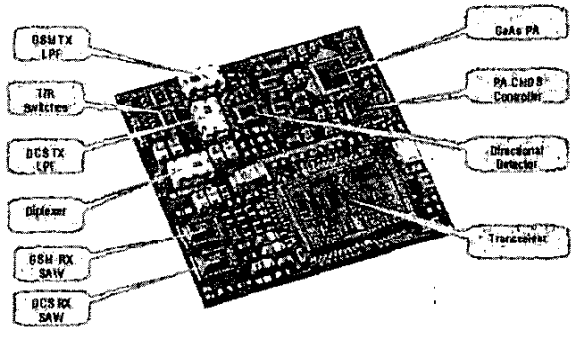

Fig. 1 SPR shown without overmold, showing location of components

Its overall dimensions are 13 x 13 x 1.8mm, including the plastic overmold which is not shown. Fig. 1 also shows the location of the major components. The substrate is a four-layer laminate. The assembly consists of a combination of chip-on-board with wire bonding, and reflow-soldered SMT components. Details of the layout design are discussed in [1].

Not shown is the land pattern on the bottom side of the laminate substrate. It consists of 40 land pads plus a large ground area in the center.

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III. GENERAL SYSTEM ARCHITECTURE

The block diagram of the SPR module is shown in Fig. 2. At the antenna port is a multilayer ceramic diplexer that separates the 900MHz and 1800MHz bands. Then for each band there is a SP2T GaAs PHEMT transmit/receive switch.

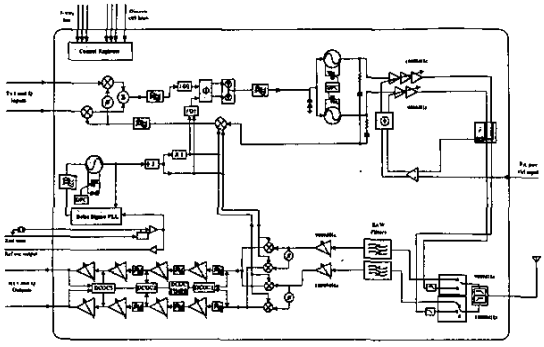

Fig. 2 SPR Block Diagram

In each receive path is placed one RF SAW filter just prior to the LNA. These SAW filters are chip-scale-packaged SMT components which are placed internal to the module. Since the receiver is a direct-conversion type, there are no post-LNA image-reject SAWs needed, but the lack of a second SAW filter for each path means that the receiver chain after the SAW must tolerate larger out-of-band blocking signals. Following these front end components, the remainder of the receiver chain resides on the BiCMOS transceiver die [2], which is the largest component visible in Fig. 1. On this die the receive path from LNA to baseband output I and Q signals is implemented. There is an LNA and quadrature-downconversion mixer for each band, then the two mixers feed the same baseband chain, which consists of several stages of gain and lowpass filtering. Receiver output signals are in the form of baseband differential I and Q. Three stages of DC offset correction are distributed through the baseband chain, from the mixer output to the end of the chain.

Also on the same BiCMOS transceiver die is the transmitter section which accepts differential baseband I and Q signals and performs quadrature modulation to drive the GaAs HBT power amplifier from a VCO. Here a quadrature modulator resides inside an upconversion phase-locked-loop. Using "crossed" I and Q signals, the modulator removes the VCO modulation to keep the loop locked to an unmodulated IF reference. There are two transmit VCOs, one for 900MHz and one for 1800MHz. These drive a two-stage 900MHz power amplifier and a three-stage 1800MHz power amplifier. Transmit power control is performed by a closed-loop system utilizing output power detection and power amplifier bias current control. The power control loop accepts an analog control voltage input.

The SPR module includes a 26MHz crystal oscillator. , though the crystal unit itself is connected externally. A fractional-N phase-locked loop uses this crystal oscillator for reference, and provides the local oscillator signals for both transmitter and receiver. There is no auxiliary PLL, as the direct-conversion receiver does not require it, and the transmitter IF is derived by division of the main local oscillator.

IV. RECEIVER

The receiver provides a gain control range of over 100dB in 2dB steps. Large gain steps (18-20dB) are provided at the LNA and mixer, and the small steps in the baseband chain. The steps are controlled via the 3-wire bus. Typically the gain is controlled (by AGC software in the DSP/μC to which the SPR interfaces) to achieve a baseband output setpoint of 30-60mVrms. At −102dBm antenna input, for instance, the voltage gain is 88dB.

The baseband filtering chain includes two real poles at the mixer output to achieve an early knockdown of blocking signals at >3MHz offset, then two more real poles plus two conjugate pole pairs for the main channel filtering. The real poles also help in keeping the group delay distortion well under 1μs over 100kHz. Overall the baseband 3dB bandwidth is 95kHz. This filtering characteristic insures that both the adjacent (200kHz) and 2^{nd}-adjacent (400kHz) interfering signals are attenuated below the desired signal. This maximizes the flexibility of this receiver regarding interface to various A/D converters with differing post-A/D digital filtering.

Since the receiver is of the direct conversion type [3], DC offsets and 2^{nd}-order distortion required close control in the design. DC offsets originating at the mixer are compensated by the aforementioned DC offset control loops in the baseband chain. DC due to local oscillator leak to the LNA input is reduced by the subharmonic mixer architecture. This also greatly reduces the extent to which local oscillator power can leak from the antenna port, as shown in baseband receiver output signal with such an intermittent (but otherwise unmodulated) blocker; blocker DC is minimal.

Fig. 3.

2^{nd}-order distortion remains low enough such that the blocking signal of the GSM AM-suppression test

produces a DC offset well under –9dBc. Characterized as 2nd-order intercept point (IP2), this equates to an input IP2 of >43dBm. This high IP2 also means the receiver is resistant to AM-modulated blockers. Fig. 4 shows a baseband receiver output signal with such an intermittent (but otherwise unmodulated) blocker; blocker DC is minimal.

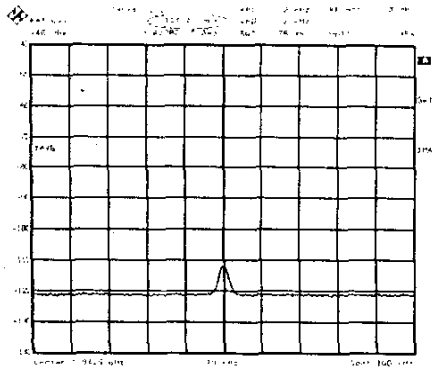

Fig. 3 RX Local Oscillator Leakage, GSM1800

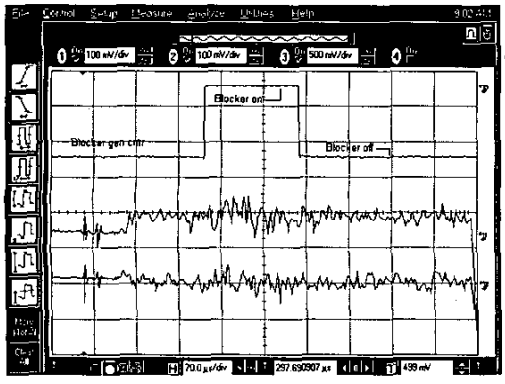

Fig. 4 RX I and Q DC result with intermittent blocker, EGSM900

V. TRANSMITTER

To help minimize the size of the SPR there is no auxiliary PLL, and the transmit IF is derived by a division of the main local oscillator, therefore the IF cannot be a fixed frequency. Rather, the IF is confined to a range of about 100MHz +/- 20MHz. This is accomplished by the use of independent programmable dividers at the phase detector input. To allow these to be independent, the modulator is placed inside the loop, such that its output is unmodulated. The flexibility in the divide ratios allows for both the minimization of the IF range and the avoidance of spurious-prone local oscillator frequencies.

As with any GSM upconversion loop transmitter, the intent is to minimize receive-band noise with little or no filtering in the transmit chain. Here the transmit VCOs put out enough power to drive the two-stage 900MHz PA and 3-stage 1800MHz PA (typically 11dBm and 7dBm respectively). At each transmit burst the VCO is first centered by a digital frequency centering loop which switches in additional tank capacitance, before the upconversion PLL begins to lock. This makes it possible for one VCO to cover the range of 824-915MHz and the other 1710-1910MHz.

The SPR transmit output power is suitable for mobile EGSM900 class 4 (2W) and GSM1800 class 1 (1W). Power is controlled by a power-sensing loop which uses a GaAs combined directional coupler and detector. The power ramp is shown in Fig. 5.

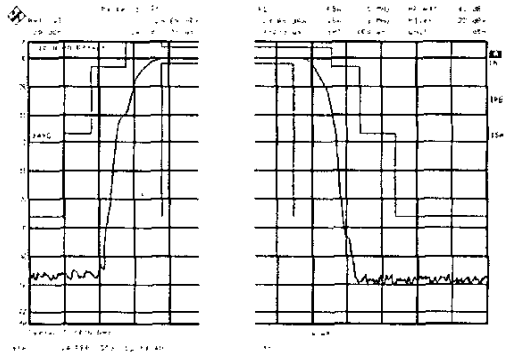

Fig. 5 Transmit Power Ramp, GSM1800

A transmit phase error measurement is given in Fig. 6.

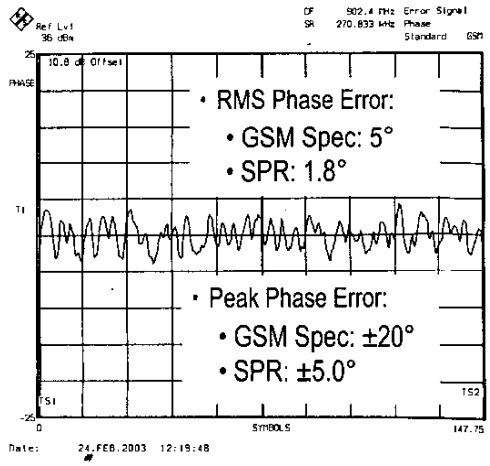

Figure 6 Transmit phase error, EGSM900, 5°/div

VI. LOCAL OSCILLATORS

All local oscillator signals on the SPR are derived from a single UHF oscillator, which is referenced to the crystal oscillator. Tuning for the crystal oscillator includes both coarse digital tuning via a capacitor array, and fine analog tuning via a varactor. Normally the coarse tuning is used for calibration/centering, while the fine tuning is used for automatic frequency control. Coarse tuning is controlled over the 3-wire bus while analog tuning utilizes an external analog input.

The UHF oscillator operates over a very wide frequency range, which is made possible by the use of digital frequency centering as already described regarding the transmit VCO. The UHF oscillator is divided and multiplied as necessary to drive the subharmonic receiver mixer. For the transmitter a similar scheme is employed to drive the upconversion loop mixer.

Loop bandwidth of the UHF PLL is about 30kHz. Including the DFC process, the UHF PLL settles in under 200μs, which makes the SPR suitable for multislot GPRS operation. Typical phase noise is shown in Fig. 7.

VII. SYSTEM INTEGRATION

At the front end of the SPR, the T/R switch function is performed by GaAs PHEMT switches. On the transmit side each switch is preceded by a multilayer ceramic lowpass filter for harmonic attenuation, and the switches themselves are low in harmonic generation. They do

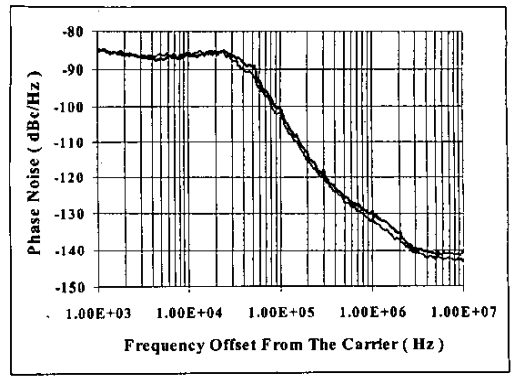

Fig. 7 UHF PLL phase noise, VCO at 1375MHz and 1500MHz

require a decoder, and this is integrated in CMOS along with the power amplifier base current driver.

The power supply arrangement is such that the battery voltage is brought in directly for the power amplifier, while regulated supplies are used elsewhere. Power supply filtering is integrated on the module.

The interface consists of 3-wire bus, enables for transmitter/receiver/synthesizer, analog controls for power amplifier control and crystal tuning, and the analog baseband differential I and Q signals for transmit and receive.

VIII. CONCLUSION

A complete GSM-specification-compliant Single Package Radio (SPR) for EGSM900/GSM1800 has been presented. It makes use of multiple semiconductor and packaging technologies to condense the complete GSM radio into a 13 x 13 x 1.8mm space.

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